Electronic Version
Stylesheet Version v1.1.1

Description

[METHOD OF ASSEMBLING PASSIVE COMPONENT]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 91137426, filed on Dec. 26, 2002.

BACKGROUND OF INVENTION

[0002] Field of Invention

[0003] The present invention relates to a semiconductor packaging technique. More particularly, the present invention relates to a method of assembling a passive component on the surface of a chip.

[0004] Description of Related Art

[0005] As semiconductor fabrication technique continues to progress, more precise and advance electronic devices are developed due to market demand. At present, popular techniques for packaging semiconductor devices include flip-chip assembly, integrated substrate design and pas-

sive component assembly.

[0006] Semiconductor production includes providing a wafer and forming highly integrated circuit on the active surface of the wafer. The active surface further includes a plurality of bonding pads thereon. Thereafter, the wafer is diced up into a plurality of dies. The die is subsequently wire-bonded or flip-chip-bonded to a carrier such as a lead frame or a substrate. The bonding pads on the die are re-distributed to the periphery or a region over the active surface of the die through transmission circuits and con-tact points on the carrier.

[0007] To meet the requirements in an integrated circuit (IC) de-sign, passive components are often attached to substrate surface using surface mount technology (SMT). Hence, the passive component is able to connect electrically with the die through the patterned circuit in the substrate. Ulti-mately, signals produced by the die are transmitted through the patterned circuit and passive component to an external electronic device.

[0008] Note that the shorter the signal transmission path be-tween the passive component and the die, the shorter will be the resistor-capacitor (RC) delay and hence raise over-all electrical performance of the die and the passive com-

ponent. Therefore, finding the shortest signal transmission path linking a passive component to the die is an important research issue.

SUMMARY OF INVENTION

[0009] Accordingly, one object of the present invention is to provide a method of assembling a passive component directly onto the surface of a die so that signal transmission path between the die and the passive component is shortened and corresponding transmission delay is reduced.

[0010] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of assembling a passive component on a die with an active surface. The passive component has a plurality of electrodes located on the periphery and the die has a plurality of bonding pads on the active surface. The method of assembling the passive component onto the die includes the following steps. An under-bump-metallurgy (UBM) layer is formed over the bonding pads. A solder block is formed on the UBM layer. And, the terminal electrodes of the passive component are bounded to the solder block. Optionally, a patterned dielectric layer can be formed over the active surface with openings to expose

the bonding pads. Optionally, a RDL can be formed to electrically couple to the bonding pads, or the UBM layer can further include the RDL.

[0011] This invention also provides chip package structure that comprises a substrate, a die, at least one under-bump-metallurgy layer, a plurality of solder blocks, a passive component, a plurality of conductive wires and a packaging plastic. The substrate has an upper surface. The die has an active surface and a back surface. The back surface of the die is in contact with the upper surface of the substrate. The active surface of the die is implemented with a plurality of boding pads thereon. The under-bump-metallurgy layer is positioned over the bonding pads. The solder blocks are placed above the under-bump-metallurgy layer. The electrodes of the passive component are bounded to the under-bump-metallurgy layer through the solder blocks. The conductive wires connect the die and the substrate together. The packaging plastic encloses the die, the passive component and the conductive wires. Optionally, a patterned dielectric layer can be included, wherein the patterned dielectric layer has openings to expose the bonding pads. Optionally, a RDL can be included to electrically couple to the bonding pads,

or the UBM layer can further include the RDL.

[0012] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0013] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0014] Figs. 1 and 2 are schematic sectional view showing the steps for assembling a passive component on a die according to one preferred embodiment of this invention.

[0015] Fig. 3 is a sectional view of a wire-bonded chip package having an assembled passive component therein according to one preferred embodiment of this invention.

Detailed Description

[0016] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever

possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0017] Figs. 1 and 2 are schematic sectional view showing the steps for assembling a passive component on a die according to one preferred embodiment of this invention. As shown in Fig. 1, a patterned dielectric layer 114 is formed on the active surface 110a of a die 110. Thereafter, photolithographic and etching processes are carried out to form openings 114a in the dielectric layer 114. The openings 114a are located in positions corresponding to the bonding pads 112 on the die 110. Thus, the openings 114a expose all the bonding pads 112. Here, the dielectric layer 114 is an option of the invention as an example, and is not the required elements or processes. An under-bump-metallurgy layer 116 is formed over each bonding pad 112 by conducting electroplating, sputtering and evaporation coating. The steps for forming the under-ball-metallurgy layers 116 include forming a metallic layer over the bonding pads 112 and the dielectric layer 114 globally and then patterning (through photolithographic and etching processes) the metallic layer. The under-bump-metallurgy layer 116 can have a multi-layered

structure that includes a stack of different metallic layers.

[0018] As shown in Fig. 2, solder blocks 118 are inserted into the openings 114a above the under-ball-metallurgy layer 116 by dip coating or printing. The solder blocks 118 are fabricated using a material such as lead-tin alloy. Finally, a passive component 120 is bonded to the solder blocks 118. The passive component 120, such as a resistor, a capacitor or an inductor, has two ends each having at least one electrode 122. Each electrode 122 is bonded to one of the solder blocks 118. Through the solder blocks 118, the electrode 122 and the bonding pad 112 on the die 110 are electrically connected. To increase bonding strength between the electrode 122 and the solder blocks 118, an additional reflow process is preferably conducted to obtain the consequent structure 126 as shown in Fig. 2.

[0019] Fig. 3 is a sectional view of a wire-bonded chip package having an assembled passive component therein according to one preferred embodiment of this invention. As shown in Fig. 3, the upper surface 102 of the substrate 100 has a die 110. The die 110 has an active surface 110a and a corresponding back surface 110b. The back surface 110b of the die 110 is attached to the upper surface 102 of the substrate 100. The dielectric layer constituting the

substrate 100 may be fabricated from a ceramic material or an organic material. The active surface 110a of the die 110 has a plurality of bonding pads 112. The bonding pads 112 can be electrically coupled to a re-distribution layer (RDL). As can be known by the skilled artisans, the RDL is used to re-redistribute the connection terminal pads of an IC to the proper positions for easy packaging. The use of RDL is optional and the RDL can be formed by an additional layer or formed by integrating in the UBM layer, wherein the UBM also provides the function of RDL. However, the RDL does not affect the features of the invention. Then, the bonding pads 112 are fabricated using aluminum or copper, for example. It should be noted that the passive component 120 (inside circle A) and the die 110 are assembled and electrically connected together through the bonding pad 112 on the active surface 110a.

[0020] According to the passive component assembling method and wire-bonded chip package as shown in Figs. 1, 2 and 3, passive components 120 may be assembled to the surface of a wafer before dicing the wafer into single dies. Thereafter, the dies are individually attached to a substrate 100 and enclosed to form a package as shown in Fig. 3. The process includes providing a wafer (containing

many undiced dies) with a plurality of bonding pads 112 on the active surfaces 110a and then forming the dielectric layer 114, the under-bump-metallurgy layers 116 and the solder blocks 118 as described with reference to Figs. 1 and 2. Thereafter, the electrodes 122 of the passive components 120 are bonded to the respective solder blocks 118. Hence, the active surface 110a of the wafer (with undiced die 110 thereon) has a plurality of passive components thereon. Consequently, the wafer is diced to produce single dies.

[0021] In Fig. 3, the die 110 is attached to the upper surface 102 of the substrate 100 with the bonding pad 104 on the die 110 electrically connected to the contact pad 108 on the substrate 100 through a conductive wire 106. Plastic materials 124 are injected to enclose the die 110, the passive component 120 and the conductive wires, thereby forming a wire-bonded chip package 130.

[0022] In summary, major advantages of the passive component assembling method according to this invention include: 1. A passive component is directly attached to the active surface of a die so that signal transmission path between the die and the passive component is shortened and corresponding transmission delay is reduced. 2. By attaching

the passive component onto the active surface of a die directly, the number of transmission circuits and contact points in the substrate for connecting between the die and the passive component is reduced. Hence, size of the substrate can be reduced. 3. Passive components can be assembled to the active surface of a wafer in a single operation after complete fabrication of the wafer. This speeds up and simplifies the process of attaching a die to a substrate.

[0023] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.